IN THE CLAIMS:

Please cancel claims 35-36 and 38-41 in the application:

1-7. (Cancelled).

8. (Previously Presented) A field effect transistor comprising:

a silicon substrate;

a gate stack on a top surface of said silicon substrate;

a recess in said silicon substrate at said top surface adjacent said gate stack;

an epitaxial silicon halo layer in said recess on said silicon substrate; and,

an epitaxial silicon source/drain layer in said recess on said epitaxial silicon halo layer,

wherein said silicon substrate comprises an oxidized portion bordering said recess directly adjacent said epitaxial silicon halo layer and wherein said oxidize portion has an oxygen content below an amount which would prevent epitaxial growth of said epitaxial silicon halo layer from said oxidized portion and further above an amount required to substantially limit dopants within said epitaxial silicon halo layer and said eptiaxial silicon source/drain layer from moving into said silicon substrate.

9. (Previously Presented) The field effect transistor in claim 8, wherein source/drain dopants are substantially limited to said epitaxial silicon source/drain layer.

10. (Cancelled).

11. (Previously Presented) The field effect transistor in claim 8, wherein said silicon substrate includes a column portion adjacent said epitaxial silicon halo layer and said epitaxial silicon source/drain layer, wherein said column portion is below said gate stack.

12. (Previously Presented) The field effect transistor in claim 9, wherein halo dopants are substantially limited to said epitaxial silicon halo layer and wherein said halo dopants are different from said source/drain dopants.

13. (Previously Presented) The field effect transistor in claim 8, further comprising isolation regions in said epitaxial silicon layer and said silicon substrate.

14. (Previously Presented) The field effect transistor in claim 8, wherein said top surface is essentially damage and native oxide free.

15-41. (Cancelled).

42. (Previously Presented) A field effect transistor comprising:

a silicon substrate;

a gate stack on a top surface of said silicon substrate;

a recess in said silicon substrate at said top surface adjacent said gate stack; and

an epitaxial silicon layer in said recess on said silicon substrate, grown from said silicon substrate and comprising dopants,

wherein said silicon substrate comprises an oxidized portion bordering said recess directly adjacent said epitaxial silicon layer and wherein said oxidized portion has an oxygen content below an amount which would prevent epitaxial growth of said epitaxial silicon layer from said oxidized portion and further above an amount required to substantially limit said dopants within said epitaxial silicon layer from moving into said silicon substrate.

43. (Cancelled).

44. (Previously Presented) The field effect transistor in claim 42, wherein said silicon substrate includes a column portion adjacent said epitaxial silicon layer, wherein said column portion is below said gate stack.

45. (Previously Presented) The field effect transistor in claim 42, wherein said top surface is essentially damage and native oxide free.

46. (Previously Presented) The field effect transistor in claim 42, wherein said epitaxial silicon layer comprises an in-situ doped epitaxial silicon source/drain layer.

47. (Previously Presented) The field effect transistor in claim 42, further comprising isolation regions in said epitaxial silicon layer and said silicon substrate.